ABSTRACT OF THE DISCLOSURE

To provide a semiconductor memory device that suppresses a terminal leak current in a test operation mode. The present invention has the following feature. For suppressing the terminal leak current in the operation mode, a layout is adopted in which a polysilicon layer overlaps with an end of a drain, the layer forming a gate electrode of a protective transistor for protecting an IC when being subjected to an electrostatic noise, the protective transistor being connected to an external terminal for the test operation mode. Consequently, a breakdown voltage of an electrostatic breakdown voltage protective transistor is increased.